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Remarks

Claims 1-2 and 4-35 are pending. By this Amendment, claims 1-2, 4-9, 11-19, 21-28, and 30-35 have been amended and claim 3 has been cancelled. No new matter is believed added. Reconsideration and allowance are requested in view of the above amendments and the following remarks.

The specification has been amended to correct the typographical error pointed out by the Examiner.

The claims have been amended for clarification under 35 U.S.C. 112, second paragraph.

Claims 1-35 are rejected under 35 U.S.C. 102(b) in view of Schrenk (US 4,910,707). This rejection is defective because Schrenk fails to teach each and every feature of the claims as required by 35 U.S.C. 102(b).

Claim 1 recites:

“A circuit arrangement (100) for protecting a chip arrangement (200), comprising:
at least one optosensitive detector unit (10), comprising at least one bipolar transistor, whose output voltage (V_{out}) is a measure of the incidence of light (Li) on the detector unit (10),
and

at least one comparator unit (20) preceded by the detector unit (10) provided for comparing the output voltage (V_{out}) of the detector unit (10) with a reference voltage (V_{ref}), wherein the data and/or functions of the chip arrangement (200) to be protected can be temporarily or permanently obstructed and/or erased (L) and/or blocked (S) and/or interrupted in the case of a failure message occurring during comparison of the output voltage (V_{out}) of the detector unit (10) with the reference voltage (V_{ref}).”

Schrenk fails to disclose, among other features, “at least one optosensitive detector unit (10), **comprising at least one bipolar transistor**, whose output voltage (V_{out}) is a measure of the incidence of light (Li) on the detector unit (10).” On the contrary, Schrenk discloses that the radiation-sensitive sensors 8 comprises photo-diodes (col. 2, lines 59-61) or a photo-resistor 14 (col. 3, lines 23-26).

In section 4 of the above-referenced Office Action, the Examiner makes several incorrect

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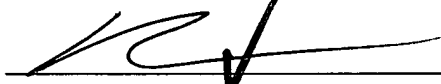
and confusing statements. For example, the Examiner asserts that the claimed "bipolar transistor" is disclosed in col. 4, lines 5-15 and FIG. 4. This is incorrect. In particular, in col. 4, lines 5-15 and FIG. 4, Schenk discloses the construction of a pn-diode photo-diode 8, not the formation of a bi-polar transistor. The Examiner also incorrectly equates the claimed emitter and collector of the claimed bipolar transistor with the self-conducting FET transistor 15 and FET transistor 16, respectively, of Schenk. Further, the Examiner asserts that the claimed comparator unit of the present invention corresponds with the programming line 4 of Schenk's memory area 1a. It is not clear how Schenk's programming line 4 can perform the claimed comparison of the "output voltage (V_{out}) of the detector unit (10) with a reference voltage (V_{ref})" as claimed. If the Examiner wishes to maintain the rejection, clarification of the Examiner's rejection is therefore respectfully requested.

Applicants respectfully submit that claims 1-2 and 4-35 are allowable because Schrenk fails to teach each and every feature of the claims as required by 35 U.S.C. 102(b).

If the Examiner believes that anything further is necessary to place the application in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number listed below.

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Respectfully submitted,



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